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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/989,563	11/19/2001	Joseph C. Sher	MICRON.113C1	2553

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EXAMINER

TRA, ANH QUAN

ART UNIT

PAPER NUMBER

2816

DATE MAILED: 01/15/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/989,563

Applicant(s)

SHER ET AL.

Examiner

Quan Tra

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 November 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

Double Patenting

1. Claims 1-25 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 17-23, 26, 33, 34, and 36-39 of Application No. 09/387,263. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are both recite the same scope.

Claim Rejections - 35 USC § 112

2. Claims 22-24 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification fails to teach the step of “irreversibly by passing at least one of the plurality of voltage control elements”.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 22-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claim 22 is misdescriptive and renders the claim ~~in~~definite. It is misdescriptive for reciting “irreversibly by passing at least one of the plurality of voltage control elements”.

Figure 4A shows “reversibly” by passing at least one of the plurality of voltage control elements by transistors 425 and 430.

Claims 23 and 24 are rejected as including the indefinite of claim 22.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Javanifrad et al. (USP 5483486, Applicant submitted IDS) in view of Furumochi (USP 5473277, Applicant submitted IDS).

As to claim 1, Javanifrad et al. shows in figure 14 a circuit comprising: a reference circuit (316); a voltage regulator (318) electrically coupled to the reference circuit which generates a first control signal (REG); a charge pump (320) which receives the control signal from the voltage regulator, the charge pump generating the test supply voltage (Vout). Thus, figure 14 shows all limitations of the claim except for the reference having a plurality of voltage regulation devices and at least one bypass device connected to at least one of the plurality of voltage regulation devices. However, Furumochi's figure 5 shows a reference circuit having plurality of voltage regulation devices (T1-T4) and at least one bypass device (SW0) connected to at least one of the plurality of voltage regulation devices. Furumochi's circuit having the advantage of varying the voltage level at the output node (OUT). Thus, it would have been obvious to one having ordinary skill in the art to use Furumochi's figure for Javanifrad et al.'s reference circuit for the purpose of generating a variable reference voltage, therefore controlling the output level of the charge pump. Thus, with the combination, it is inherent that the at least one bypass device is activated following the certification of the semiconductor device to bypass the at least one of

Art Unit: 2816

the plurality of voltage regulation devices from the clamp circuit to lower the clamping threshold of the clamp circuit, the voltage regulator generating a second control signal responsive to the lowered clamping threshold of the clamp circuit to cause the charge pump to generate the operational supply voltage.

As to claim 2, Furumochi's figure 5 shows the plurality of voltage regulation devices comprise diodes.

As to claim 3, Furumochi's figure 5 shows the diodes are implemented through transistors.

As to claim 4, Furumochi's figure 5 further shows the bypass device comprising a fuse (FU) in series with a transistor (TN4).

As to claim 5, Furumochi's figure 5 shows bypass device is activated by blowing the fuse.

As to claim 6, with the combination of the prior arts, it is inherent that value of the operational supply voltage is reduced for each voltage regulation device bypassed.

As to claim 7, with the combination of the prior arts, it is inherent that the voltage regulation devices limit the maximum voltage output of the clamp circuit.

As to claim 8, with the combination of the prior arts, it is inherent that the first control signal reduces the test supply voltage when the voltage regulation devices limit the output of the clamp circuit.

As to claim 9, with the combination of the prior arts, it is inherent that the second control signal reduces the operational supply voltage when the non-bypassed voltage regulation devices (T1, T2..) limit the output of the clamp circuit.

Claims 10-21 and 25 recite similar limitations of claims 1-9. Therefore, they are rejected for the same reasons.

Insofar as understood to claim 22, the prior arts fails to teach the step of reversibly bypassing at least one of the plurality of voltage control elements; establishing a third voltage control signal during a third period from the plurality of voltage control elements which are not reversibly bypassed; and generating a third supply voltage from the third voltage control signal. However, it is seen as an design choice and obvious to one having ordinary skill in the art to bypass Furumochi's another diode for the purpose of further reducing the output voltage level (OUT).

As to claim 23, Furumochi's figure 5 shows reversibly bypassing at least one of the plurality of voltage control elements comprises blowing a fuse.

As to claim 24, it is seen as an obvious design choice for reversibly bypassed the diode after testing of the semiconductor device dependent upon particular environment of use to ensure optimum performance.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

Art Unit: 2816

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QT

QT
January 10, 2002

Toan Tran

Toan Tran
Primary Examiner